Chapter 1

Appendix A

Appendix C

c.3 Simple implementation of RISC-V

c.1 up to page c.14

Amdahl’s Law

before opt : (1-f)

timeout doing optimized part BEFORE speedup : f

speedup to optimized part : S

Processor Performance Equation

Definition of speed up

Design

RISC vs CICS

Instruction set design

PDP-8

8080

RISC-V

VHDL

2’s complement

invert

add 1